Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the above-identified application.

Listing of Claims

1-27. Cancelled.

28. (**Currently Amended**) A method comprising:

issuing an instruction to transfer data between a memory and a processor, wherein the data comprises a plurality of data elements each having a data width, and wherein the plurality of data elements are stored in non-contiguous locations in the memory;

transferring the data between the memory and the processor via a memory bus coupled therebetween, wherein the data is transferred two or more data elements at a time.

29. (Previously Presented) The method of claim 28 further comprising:

determining an ending address of the data to be transferred from a starting address contained in the instruction and the data width;

generating an address exception when it is determined that the data to be transferred crosses a page boundary of a page in the memory.

30. (Previously Presented) The method of claim 29 wherein:

the instruction comprises a length of the data to be transferred and a stride of the data to be transferred;

wherein determining the ending address comprises:

multiplying the stride and the data width to provide a first result;

subtracting one from the length to provide a second result;

multiplying the first result and the second result to provide a third result; and

adding the third result to the starting address to provide the ending address.

31. (Previously Presented) The method of claim 28 further comprising:

transferring the data to be transferred between the memory and the processor via a burst transfer.

32. (Previously Presented) The method of claim 29 further comprising:

interrupting the data transfer in response to generating the address exception.

33. **(Currently Amended)** A computer readable medium comprising instructions executable by a computer system, wherein the computer system performs a method in response to executing the instructions, the method comprising:

determining a quantity of data elements to be transferred in parallel between a memory and a processor via a memory bus coupled therebetween, wherein the quantity is determined from a width of the data elements to be transferred and a width of the memory bus, and wherein the data elements are stored in non-contiguous locations in the memory;

initiating a transfer of the quantity of data elements between the memory and the processor.

34. (Previously Presented) The computer readable medium of claim 33 wherein the method further comprises:

determining an ending address of data to be transferred between the memory and the processor via the memory bus, wherein the data includes the quantity of data elements, wherein the ending address is determined from a starting address of the data and the width of the data elements;

generating an address exception when it is determined that the data to be transferred crosses a page boundary of a page in the memory.

35. (Previously Presented) The computer readable medium of claim 34 wherein determining the ending address comprises:

multiplying a stride of the data to be transferred and the width of the data elements to provide a first result;

subtracting one from a length of the data to be transferred to provide a second result;

multiplying the first result and the second result to provide a third result; and

adding the third result to the starting address to provide the ending address.

36. (Previously Presented) The computer readable medium of claim 34 wherein the method further comprises:

transferring the data to be transferred between the memory and the processor via a burst transfer.

37. (Previously Presented) The computer readable medium of claim 34 wherein the method further comprises:

interrupting the data transfer in response to generating the address exception.

38. (Previously Presented) The computer readable medium of claim 37 wherein the method further comprises:

performing a burst transfer of the stream of data from the memory to the buffer of the processor, the burst transfer bypassing a data cache of the processor.

39. (**Currently Amended**) An apparatus comprising:

a memory;

a processor coupled to the memory;

a circuit coupled to the processor, wherein the circuit is configured to calculate a quantity of data elements to be transferred between the memory and the processor via a memory bus coupled therebetween, wherein the circuit calculates the quantity from a width of the data elements and a width of the memory bus, and wherein the data elements are stored in non-contiguous locations in the memory.

40. (Previously Presented) The apparatus of claim 39 wherein the circuit is configured to generate an ending address of data to be transferred between the memory and the processor via the memory bus, wherein the circuit generates the ending address from a starting address of the data to be transferred and the data width of the data elements, wherein the data includes the data elements, and wherein the circuit generates an address exception when it is determined that the data to be transferred crosses a page boundary of a page in the memory.

41. (Previously Presented) The apparatus of claim 40 wherein the circuit generate data width to provide a first result;

subtracting one from a length of the data to be transferred to provide a second result;

multiplying the first result and the second result to provide a third result; and

adding the third result to the starting address to provide the ending address.